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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,312	12/15/2003	Naoki Makita	70404.12	1687

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,312	MAKITA, NAOKI	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18-20,22-37 and 55-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,3,5,7,9,11,13,18-20,23,26,27,30,31,35-37,57 and 58* is/are allowed.

6)☒ Claim(s) *1,4,6,8,10,12,14-16,22,24,25,28,29,32-34,55 and 56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/27/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of Group I, claims 1-3 and 55-58, in the reply filed on 7/20/05 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (US 2002/0102823 A1) in view of Murakami et al. (US 2002/0068388 A1).

Yamaguchi et al. teach in figure 4 a semiconductor device comprising a thin film transistor including a semiconductor layer 9 (labeled in figures 2 and 3, unlabeled in figure 4) that includes a channel region 13 (on left side), a source region and a drain region 14, a gate insulating film 5 provided on the semiconductor layer, and a gate electrode 6 for controlling a conductivity of the channel region, wherein a surface of the semiconductor layer includes a protruding portion, and a side inclination angle of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer. As shown, the gate electrode has a side inclination angle of approximately 90 degrees.

Yamaguchi et al. further teaches a cross-section of the gate electrode including first and second opposing sides that are parallel to each other (top and bottom sides) but does not teach a third side that is not parallel to any other side of the cross-section of the gate electrode.

Murakami et al. teach in figures 4b and 4c, as well as in finished product 6c, a thin film transistor that includes a channel region, source region, drain region, gate insulating film, and a gate electrode (labeled 310b in figure 4b and 315b in figure 4c) Murakami et al. teach the gate electrode 315b having a cross-section including first and second opposing sides that are parallel to each other (top and bottom sides) and a third side that is not parallel to any other side of the cross-section of the gate electrode (left or right side of the tapered gate). Murakami et al. teach throughout figures 4b-5a and in paragraphs [0106] and [0112]-[0115] that the tapered gate electrode is used in an implantation process to form LDD regions.

Yamaguchi et al. and Murakami et al. are from the same field of endeavor. At the time of the invention it would have been obvious to one of ordinary skill in the art to employ the tapered gate implantation process of Murakami et al. in the device of Yamaguchi et al. The motivation for doing so is to simultaneously provide regions with different doping concentrations (such as 401 and 403 of Murakami et al.) to form LDD regions that are effective in reducing the OFF current value of the transistor. Thus, the combination of Yamaguchi et al. and Murakami et al. teach the invention of claim 1.

With regard to claim 4, as seen in figure 4 Yamaguchi et al. teach multiple protruding portions all having approximately the same side surface inclination angle less than that of the gate.

With regard to claim 6, the side surface inclination angle of the gate is about 75 to 90 degrees. Further, in the combination using the gate and implantation process of Murakami et al., the gate as taught by Murakami et al. has an inclination angle (taper angle) of nearly 90 degrees (see Murakami et al. paragraph [0114]).

With regard to claim 8, an inclination angle of the protruding portion is about 30 to about 70 degrees.

With regard to claim 10, as taught in paragraph [0076] an average height of the protruding portion is about 8 to about 60 nm.

With regard to claim 14, the semiconductor film is a crystalline film and the protruding portions are located over crystal grain boundaries.

With regard to claim 15, as can be seen in figures 3 and 4, the crystal grain boundary is a multipoint where three of more crystal grains meet.

With regard to claim 16, the diameter of the crystal grains is about 100 to about 1000 nm.

With regard to claim 22, the semiconductor layer is a crystalline layer having protrusions formed through a melting/solidification process.

With regard to claims 28 and 29, the semiconductor layer is made up primarily of regions oriented along <111> crystal zone planes wherein 50% or more of the regions are oriented along a (110) plane.

With regard to claims 55 and 56, Yamaguchi et al. teach an electronic device comprising the device of claim 1 and further teach a display section where an image is displayed by using the semiconductor device (see figure 5).

4. Claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US Patent No. 5,693,959) in view of Murakami et al. (US 2002/0068388 A1).

Inoue et al. teach in figure 1, for example, a thin film transistors as claimed in claim 1. Inoue et al. teach a semiconductor layer having protruding portions (under contacts 106a/106b) where a side inclination angle of the gate 104 is greater than an inclination angle of the protruding portions.

Inoue et al. further teaches a cross-section of the gate electrode including first and second opposing sides that are parallel to each other (top and bottom sides) but does not teach a third side that is not parallel to any other side of the cross-section of the gate electrode.

Murakami et al. teach in figures 4b and 4c, as well as in finished product 6c, a thin film transistor that includes a channel region, source region, drain region, gate insulating film, and a gate electrode (labeled 310b in figure 4b and 315b in figure 4c) Murakami et al. teach the gate electrode 315b having a cross-section including first and second opposing sides that are parallel to each other (top and bottom sides) and a third side that is not parallel to any other side of the cross-section of the gate electrode (left or right side of the tapered gate). Murakami et al. teach throughout figures 4b-5a and in

paragraphs [0106] and [0112]-[0115] that the tapered gate electrode is used in an implantation process to form LDD regions.

Inoue et al. and Murakami et al. are from the same field of endeavor. At the time of the invention it would have been obvious to one of ordinary skill in the art to employ the tapered gate implantation process of Murakami et al. in the device of Inoue et al. The motivation for doing so is to simultaneously provide regions with different doping concentrations (such as 401 and 403 of Murakami et al.) to form LDD regions that are effective in reducing the OFF current value of the transistor. Thus, the combination of Inoue et al. and Murakami et al. teach the invention of claim 1.

With regard to claim 4, Inoue et al. teach multiple protruding portions all having approximately the same side surface inclination angle less than that of the gate.

With regard to claim 6, the side surface inclination angle of the gate is about 75 to 90 degrees. Further, in the combination using the gate and implantation process of Murakami et al., the gate as taught by Murakami et al. has an inclination angle (taper angle) of nearly 90 degrees (see Murakami et al. paragraph [0114]).

With regard to claim 8, an inclination angle of the protruding portion is about 30 to about 70 degrees.

With regard to claim 10, as taught in column 6 lines 46-48 an average height of the protruding portion is about 8 to about 60 nm.

With regard to claim 22, the semiconductor layer is a crystalline layer having protrusions formed through a melting/solidification process.

With regard to claim 34, Inoue et al. teach a lightly-doped impurity region 102b/102f at a junction between the channel and the source or drain region.

With regard to claims 55 and 56, Inoue et al. teach an electronic device comprising the device of claim 1 and further teach a display section where an image is displayed by using the semiconductor device (see figures 7 or 8 for example).

5. Claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (US 2003/0080384 A1) in view of Murakami et al. (US 2002/0068388 A1).

Takahashi et al. teach in figure 5(c) a semiconductor device including a thin film transistor including a semiconductor layer 71 that has a protruding portion, an insulator 69, a gate 70, a source and drain 66, where an inclination angle of the gate is greater than an inclination angle of the protruding portion.

Takahashi et al. further teaches a cross-section of the gate electrode including first and second opposing sides that are parallel to each other (top and bottom sides) but does not teach a third side that is not parallel to any other side of the cross-section of the gate electrode.

Murakami et al. teach in figures 4b and 4c, as well as in finished product 6c, a thin film transistor that includes a channel region, source region, drain region, gate insulating film, and a gate electrode (labeled 310b in figure 4b and 315b in figure 4c) Murakami et al. teach the gate electrode 315b having a cross-section including first and second opposing sides that are parallel to each other (top and bottom sides) and a third

side that is not parallel to any other side of the cross-section of the gate electrode (left or right side of the tapered gate). Murakami et al. teach throughout figures 4b-5a and in paragraphs [0106] and [0112]-[0115] that the tapered gate electrode is used in an implantation process to form LDD regions.

Takahashi et al. and Murakami et al. are from the same field of endeavor. At the time of the invention it would have been obvious to one of ordinary skill in the art to employ the tapered gate implantation process of Murakami et al. in the device of Takahashi et al. The motivation for doing so is to simultaneously provide regions with different doping concentrations (such as 401 and 403 of Murakami et al.) to form LDD regions that are effective in reducing the OFF current value of the transistor. Thus, the combination of Takahashi et al. and Murakami et al. teach the invention of claim 1.

With regard to claim 4, Takahashi et al. teach multiple protruding portions all having approximately the same side surface inclination angle less than that of the gate.

With regard to claim 6, the side surface inclination angle of the gate is about 75 to 90 degrees. Further, in the combination using the gate and implantation process of Murakami et al., the gate as taught by Murakami et al. has an inclination angle (taper angle) of nearly 90 degrees (see Murakami et al. paragraph [0114]).

With regard to claim 12, an average surface roughness of the surface of the semiconductor layer is about 4 to about 30 nm.

With regard to claim 55, Takahashi et al. teach an electronic device comprising the device of claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 24, 25 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. with Murakami et al. as applied to claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55 and 56 above, and further in view of Yamazaki et al. (US 2002/0100937 A1).

Yamaguchi et al. teach forming their layer using a melting/solidification process but do not teach including a catalyst element capable of promoting crystallization of an amorphous semiconductor film.

Yamazaki et al. teach adding a catalyst element to a semiconductor film to promote crystallization during a melting/solidification process.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include a catalyst element in the semiconductor layer of Yamaguchi in order to promote crystallization to form a crystalline layer having excellent crystallinity.

With regard to claim 25, Yamazaki teach that the catalyst element is nickel (Ni).

With regard to claim 32, Yamaguchi et al. teaches the crystal grains having the same diameter as in the instant invention (about 100nm to about 1000nm as recited in claim 16 above) but is silent as to a "domain diameter of crystal domains." Nonetheless, the claimed range of about 2 micron to about 10 micron is considered obvious over Yamaguchi et al. in view of Yamazaki et al. It is obvious that when the

catalyst element of Yamazaki et al. is incorporated into the melting/solidification process of Yamaguchi et al. the resulting domain diameters of the semiconductor film will have the claimed diameter. As explained in paragraph [0106] of applicant's specification, when a catalyst is used (during the crystallization process) the domain diameters are typically about 2 micron to about 10 micron. Thus, applicant's specification provides evidence that when the catalyst is used the claimed domain diameter will result. Thus, even though Yamaguchi et al. and Yamazaki et al. do not explicitly teach a domain diameter, the device resulting from their combination will have the claimed domain diameter.

Allowable Subject Matter

8. Claims 2, 3, 5, 7, 9, 11, 13, 18-20, 23, 26, 27, 30, 31, 35, 36, 37, 57 and 58 are allowed.

9. The following is an examiner's statement of reasons for allowance: Prior art of record fails to teach, disclose, or suggest, either alone or in combination, the device as recited in claim 2 including a gate electrode includes a first step portion and a second step portion provided on the first step portion, and a side surface inclination angle of each of the first and second step portions is larger than an inclination angle of the protruding portion of the semiconductor layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

10. Applicant's arguments with respect to claim 1 and it's dependents have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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